

**INFORMATION DISCLOSURE CITATION**  
(Use several sheets if necessary)

Docket Number (Optional)  
**FIS9-2001-039**

Application Number  
**10/040,122**

Applicant(s)  
**SCOTT ET AL.**

Filing Date  
**01/02/02**

Group Art Unit  
**2825**

U.S. PAT. & T.M. OFF.  
10/040122

**U.S. PATENT DOCUMENTS**

| *EXAMINER<br>INITIAL | REF | DOCUMENT NUMBER | DATE     | NAME               | CLASS | SUBCLASS | FILING DATE<br>IF APPROPRIATE |
|----------------------|-----|-----------------|----------|--------------------|-------|----------|-------------------------------|
| WD                   |     | 6,256,759       | 07-03-01 | BHAWMIK ET AL.     |       |          |                               |
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**FOREIGN PATENT DOCUMENTS**

| REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation |    |
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**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

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| WD |  | "TEST POINT INSERTION FOR SCAN-BASED BIST" SEISS ET AL. PROCEEDING OF THE EUROPEAN TEST CONFERENCE, pp. 253, 1991.                                    |
| WD |  | "TESTABILITY-DRIVEN RANDOM TEST-PATTERN GENERATION" LISANKE ET AL., IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, Vol. CAD-6, Nov. 1987, pp. 1082-1087. |
| WD |  | "ON TESTABILITY ANALYSIS OF COMBINATIONAL NETWORKS" BRGLEZ ET AL, PROCEEDINGS OF INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, pp.221-225, 1984.   |
| WD |  | "ON GENERATING OPTIMAL SIGNAL PROBABILITIES FOR RANDOM TESTS: A GENETIC APPROACH", SRINIVAS ET AL. VLSI DESIGN, 1996, VOL. 4, NO.3, pp 207-215.       |
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EXAMINER

*[Signature]*

DATE CONSIDERED

**9/2003**

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.